CUSTOMER :

M O D E L : MOG-122GB03B-S Series

DESCRIPTION : LCD MODULE

◆ CUSTOMER APPROVAL

	CHECKED	CHECKED	APPROVAL
APPROVAL			
REMARK			

◆ SUPPLIER APPROVAL

PREPARED	CHECKED		APPROVAL

MYTECH CORPORATION

180 Old Tappan Rd., Bldg. 6, Old Tappan, NJ 07675
Tel: (201) 784-8867 Fax: (201) 784-8932
Email: *mysales@mytechcorp.com*

NOTE: 1. This specification may, wholly or partially, be subjected to change without notice.
2. Information contained herein is proprietary information of MYTECH CORPORATION. The dissemination use or duplication for any purpose other than for which the information is provided is prohibited by MYTECH CORPORATION except by express permission.

1. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	122x32	dots
Module dimension (W*H*T)	65.8*27.1*8.4(Max)-LED, EL B/L	mm
View area	60.5(W)x18.5(H)	mm
Dot size	0.40(W)x0.45(H)	mm
Dot pitch	0.44(W)x0.49(H)	mm

(2) Controller IC: SED1520Daa (External clock: 2KHz)

(3) Temperature Range

	Normal	Wide
Operating	0 ~+50℃	-20 ~+70℃
Storage	-10 ~+60℃	-30 ~+80℃

2. Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Unit
Logic Circuit Supply Voltage		VDD-VSS	0	8.0	V
LCD Driving Voltage		VDD-VO	0	10.0	V
Input Voltage		VI	VSS	VDD	V
Normal temp. type	Operating Temp.	TOP	0	+50	°C
	Storage Temp.	TSTG	-20	+70	°C
Wide temp. type	Operating Temp.	TOP	-20	+70	°C
	Storage Temp.	TSTG	-30	+80	°C

3. Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
----- Electronic Characteristics -----							
Logic Circuit Supply Voltage	VDD-VSS	--	4.5	5.0	5.5	V	
LCD Driving Voltage (Normal Temp. type)	VDD-VO	0 °C	--	6.9	--	V	
		25 °C	--	6.4	--		
		50 °C	--	6.0	--		
LCD Driving Voltage (Wide Temp. type)	VDD-VO	-20 °C	--	9.4	--	V	
		0 °C	--	9.0	--		
		25 °C	--	8.6	--		
		50 °C	--	8.3	--		
		70 °C	--	8.0	--		
Input Voltage	VIH	--	0.7 VDD	--	VDD	V	
	VIL	--	VSS	--	0.3 VDD	V	
Logic Supply Current	IDD	VDD = 5V	--	0.5	1.5	mA	
----- Optical Characteristics -----							
Contrast	CR	STN type	--	5	--		Note 1
		FSTN type		7			
Rise Time	tr	25°C	--	100	150	ms	Note 2
Fall Time	tf	25°C	--	120	200	ms	
Viewing Angle Range	θ f	25°C & CR≥2	--	40	--	Deg.	Note 3
	θ b		--	35	--		
	θ l		--	40	--		
	θ r		--	40	--		
Frame Frequency	fF	25°C	--	60	--	Hz	

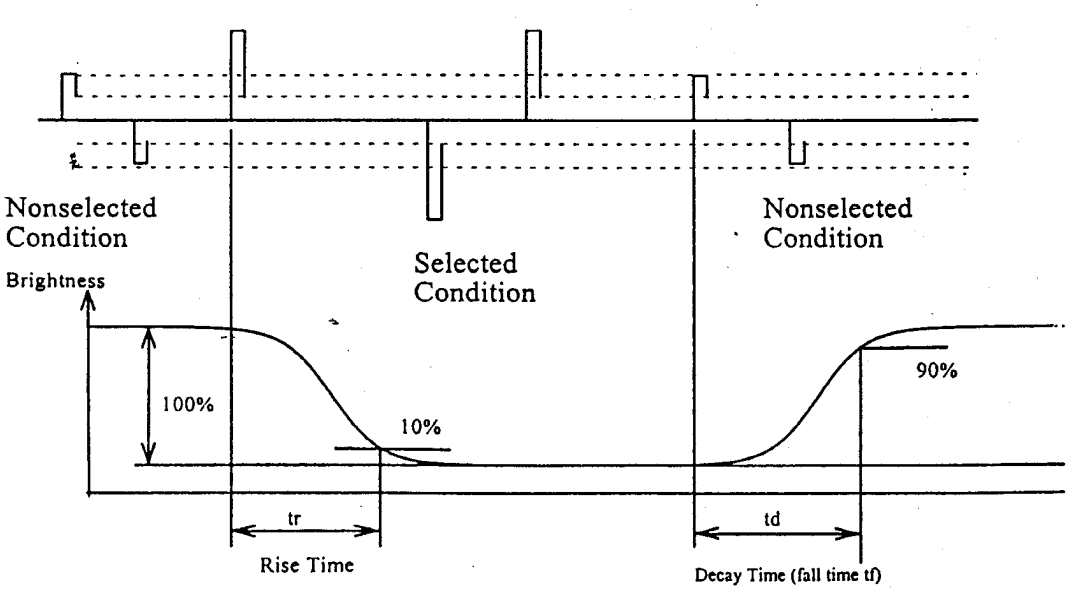
Note: 6.4V at Normal Temperature

8.6V at Wide Temperature

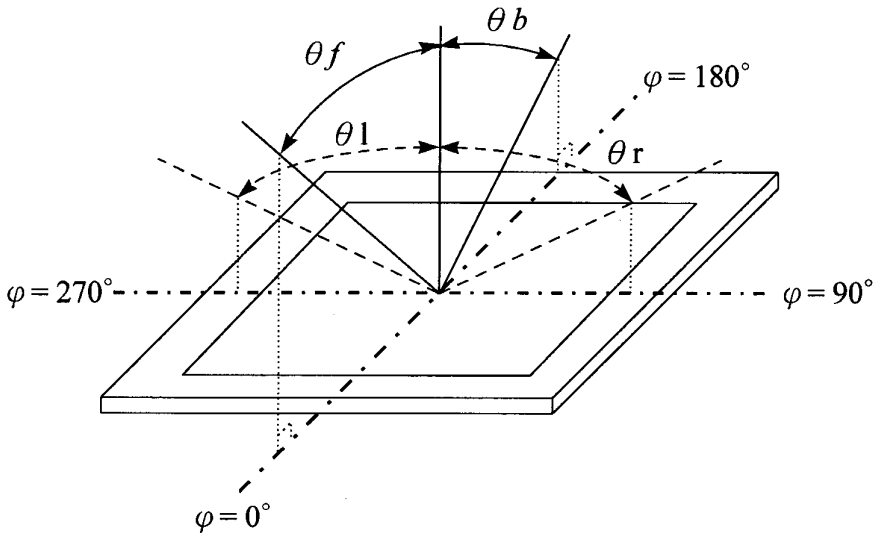
(NOTE 1) Contrast ratio :

CR = (Brightness in OFF state) / (Brightness in ON state)

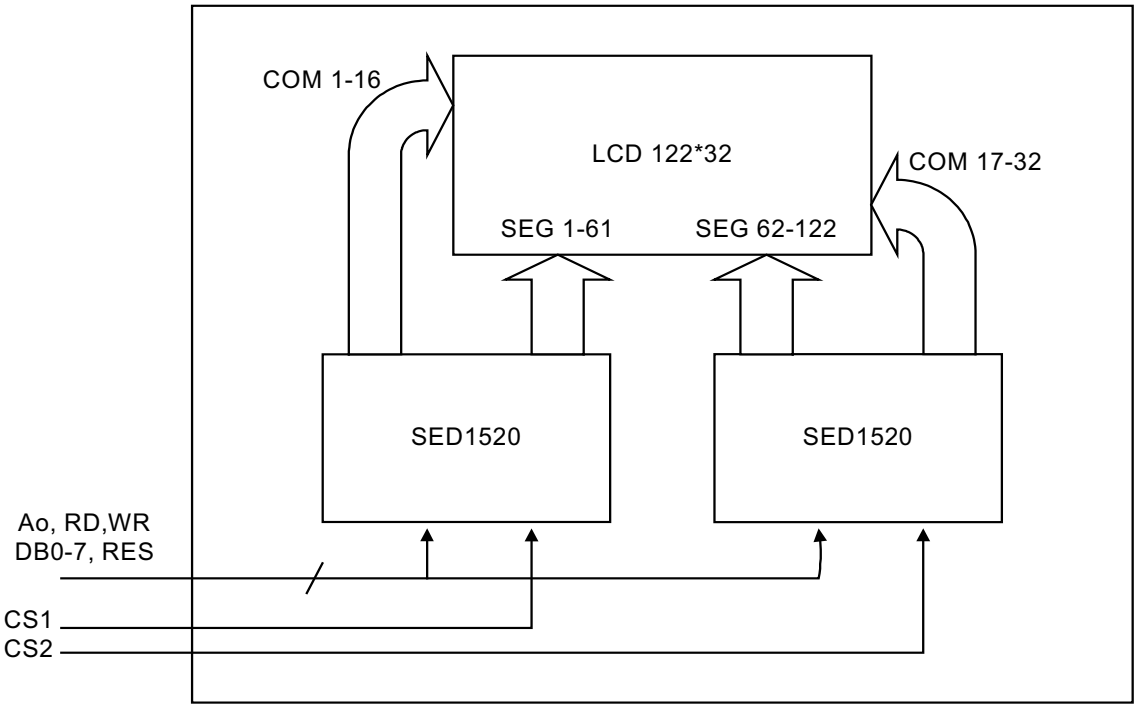
(NOTE 2) Response time :



(NOTE 3) Viewing angle



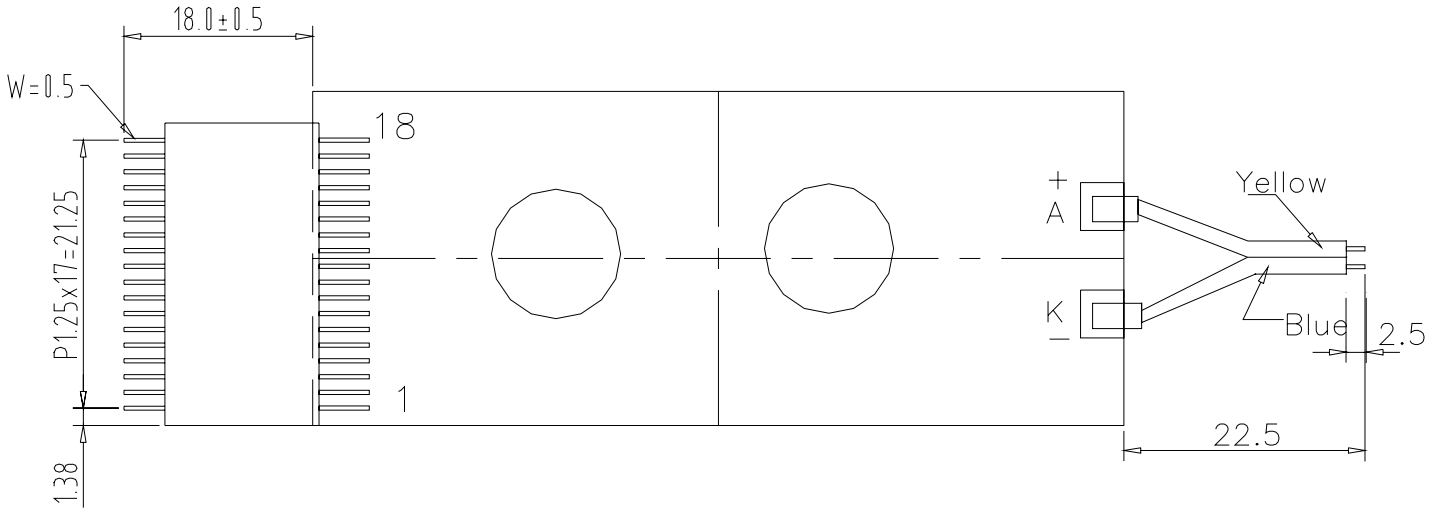
4. Block Diagram



5. Interface Pin Function

No.	Symbol	Function
1	Ao	H: Data L: Instruction
2	CS2	L: Enable chip2
3	CS1	L: Enable chip1
4	CL	External Clock 2KHz
5	RD/E	RD for 80 series , E for 68 series
6	WR(R/W)	WR for 80 series , R/W for 68 series
7	VSS	Power Supply (GND)
8-15	DB0-DB7	Data bus line
16	VDD	Power Supply (+3V ~ +5V)
17	RES	H: 68 series , L: 80 series
18	VO	Contrast Adjustment

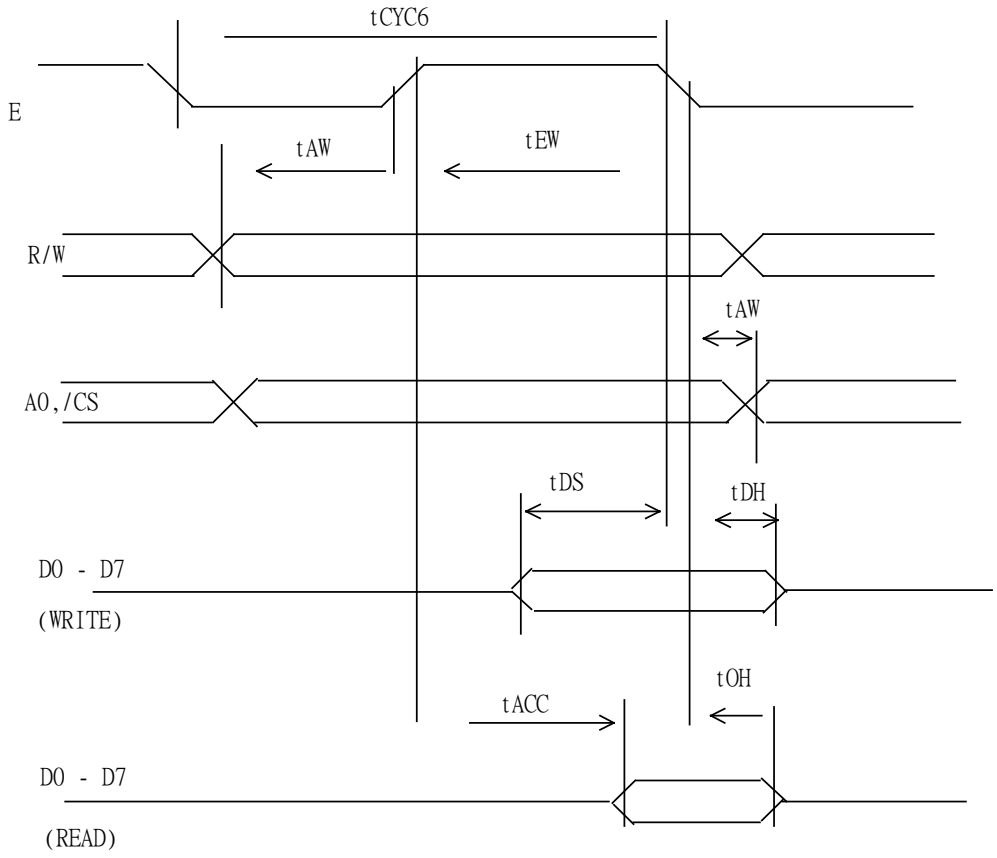
＊FFC Cable (Front transmissive view)



6. Timing Characteristics

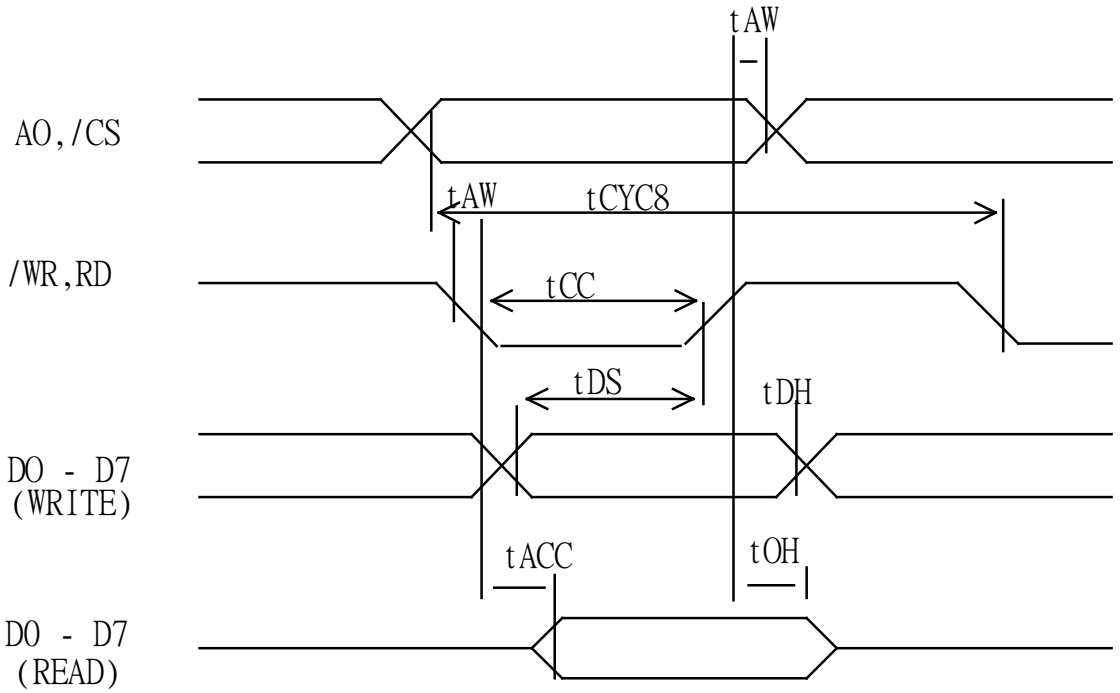
6.1 MPU Bus Read/Write (68-family MPU)

Item		Symbol	Condition	Min	Max	Unit
System Cycle Time		t_{CYC6}		1.0	--	us
Address setup time		t_{AS}		20	--	ns
Address hold time		t_{AH}		10	--	ns
Data setup time		t_{DD}		80	--	ns
Data hold time		t_{DH}		10	--	ns
Output disable time		t_{OH}	CL=100pF	10	60	ns
Access time		t_{ACC}		--	90	ns
Enable pulse width	Read	t_{EW}		100	--	ns
	Write			80	--	



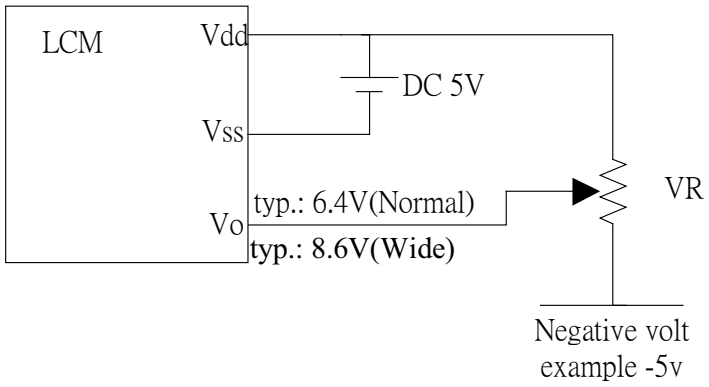
6.2 MPU Bus Read/Write (80-family MPU)

Item	Symbol	Condition	Min	Max	Unit
System cycle time	t_{CYC8}		1.0	--	us
Control Pulse Width	t_{CC}		200	--	ns
Address setup time	t_{AS}		20	--	ns
Address hold time	t_{AH}		10	--	ns
Data setup time	t_{DSW}		80	--	ns
Data hold time	t_{DH}		10	--	ns
Access time	t_{ACC}	CL=100pH	--	90	ns
Output disable time	t_{0H}		10	60	ns

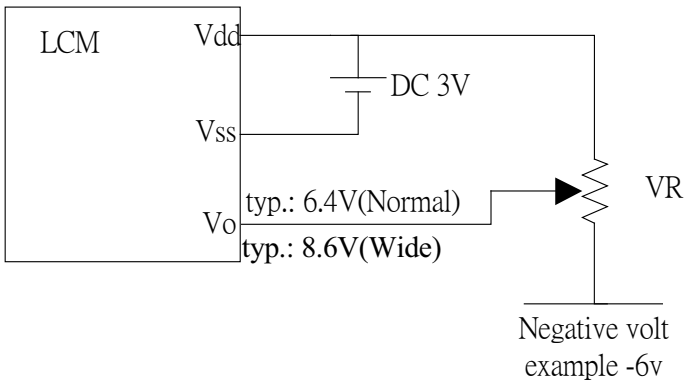


7. Power Supply for LCD Module and LCD Operating Voltage a Adjustment

＊(Option) LCM operating on " DC 5V " input with external negative voltage



＊(Option) LCM operating on " DC 3V " input with external negative voltage



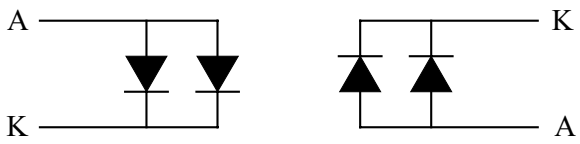
8. Backlight Information

8.1 Specification

(1) LED edge / yellow-green Ta = 25℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Forward Voltage	V_F	IF=40mA	1.9	2.1	2.3	V	Supply Voltage between A , K
Peak emission wavelength	λ P	IF=20mA	--	570	--	nm	
Spectrum radiation bandwidth	△ λ	IF=20mA	--	30	--	nm	
Reverse current	I_R	VR = 4V	--	--	0.8	mA	
* Luminous intensity	IV	IF=40mA	8	11	--	cd/㎡	
Luminous tolerance		IF=40mA	--		50	%	

* Note : Measured at the bare LED back-light unit.



Edge light
2×2= 4 (Dice numbers)

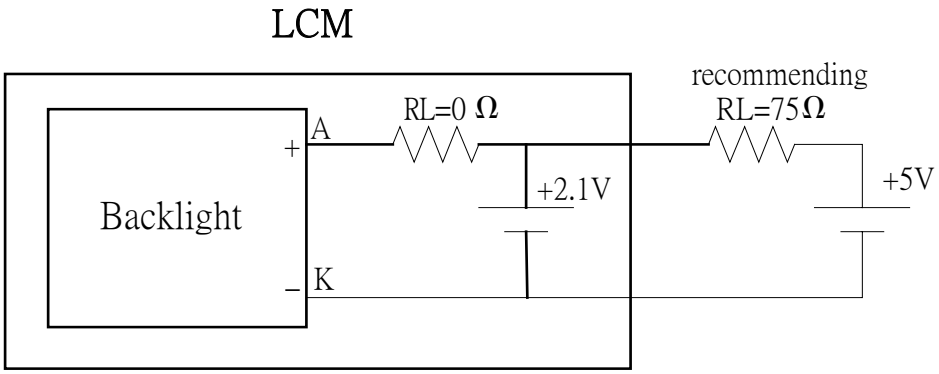
(2) EL Blue / white

Parameter	Specification	Unit
Color	Blue/White	-
Voltage	Vrms = 110	V(AC)
Frequency	Sine Wave = 400	Hz
Current Density	0.12	mA / cm^2
Bare EL Initial Brightness	40	cd / m^2
LCM Initial Brightness	13	cd / m^2

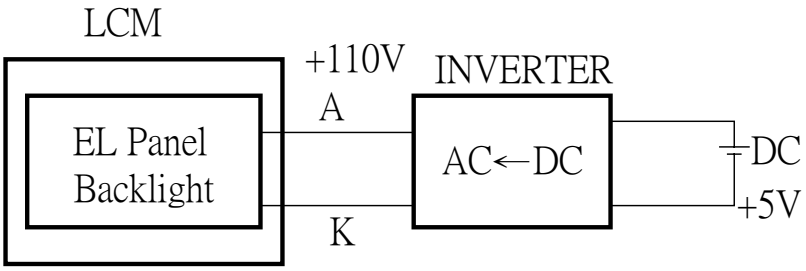
8.2 Backlight driving methods

a. LED B/L drive from A.K directly

a.1 edge / yellow-green



b. E/L B/L driven from A.K cable directly



9. Quality Assurance

9.1 Test Conditions

Tests should be conducted under the following conditions :
Ambient temperature : 25 ± 5°C
Humidity : 60 ± 25% RH.

9.2 Sampling Plan

Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

9.3 Acceptable Quality Level

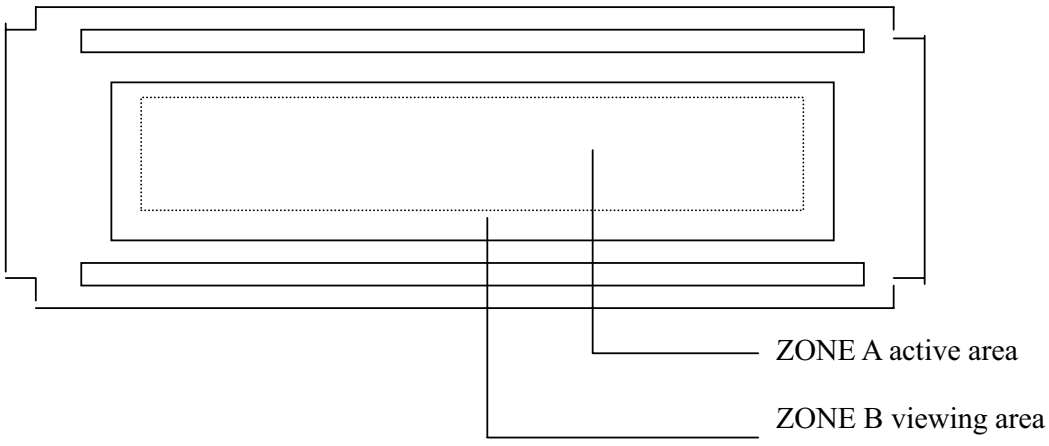
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

9.4 Appearance

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.

9.5 Inspection Quality Criteria

Item	Description of defects			Class of Defects	Acceptable level (%)
Function	Short circuit or Pattern cut			Major	0.65
Dimension	Deviation from drawings			Major	1.5
Black spots	Ave . dia . D	area A	area B	Minor	2.5
	D≤0.2	Disregard			
	0.2<D≤0.3	3	4		
	0.3<D≤0.4	2	3		
	0.4<D	0	1		
Black lines	Width W, Length L	A	B	Minor	2.5
	W≤0.03	disregard			
	0.03<W≤0.05	3	4		
	0.05<W≤0.07 , L≤3.0	1	1		
	See line criteria				
Bubbles in polarizer	Average diameter D 0.2 < D < 0.5 mm for N = 4 , D > 0.5 for N = 1			Minor	2.5
Color uniformity	Rainbow color or newton ring.			Minor	2.5
Glass Scratches	Obvious visible damage.			Minor	2.5
Contrast ratio	See note 1			Minor	2.5
Response time	See note 2			Minor	2.5
Viewing angle	See note 3			Minor	2.5



10. Reliability

Test Item	Test Conditions		Note
	Normal Temp. type	Extended Temp. type	
High Temperature Operation	50±3°C , t=96 hrs	70±3°C , t=96 hrs	
Low Temperature Operation	0±3°C , t=96 hrs	-20±3°C , t=96 hrs	
High Temperature Storage	70±3°C , t=96 hrs	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-20±3°C , t=96 hrs	-30±3°C , t=96 hrs	1,2
Temperature Cycle	-20°C ~ 25°C ~ 70°C 30 m in. 5 min. 30 min. (1 cycle) Total 5 cycle	-30°C ~ 25°C ~ 80°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Humidity Test	40 °C, Humidity 90%, 96 hrs		1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis		2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

11. Handing Precautions

(1) A LCD module is a fragile item and should not be subjected to strong mechanical shocks.

(2) Avoid applying pressure to the module surface. This will distort the glass and cause a change in color.

(3) Under no circumstances should the position of the bezel tabs or their shape be modified.

(4) Do not modify the display PCB in either shape or positioning of components.

(5) Do not modify or move location of the zebra or heat seal connectors.

(6) The device should only be soldered to during interfacing. Modification to other areas of the board should not be carried out.

(7) In the event of LCD breakage and resultant leakage of fluid do not inhale, ingest or make contact with the skin. If contact is made rinse immediately.

(8) When cleaning the module use a soft damp cloth with a mild solvent, such as Isopropyl or Ethyl alcohol. The use of water, ketone or aromatic is not permitted.

(9) Prior to initial power up input signals should not be applied.

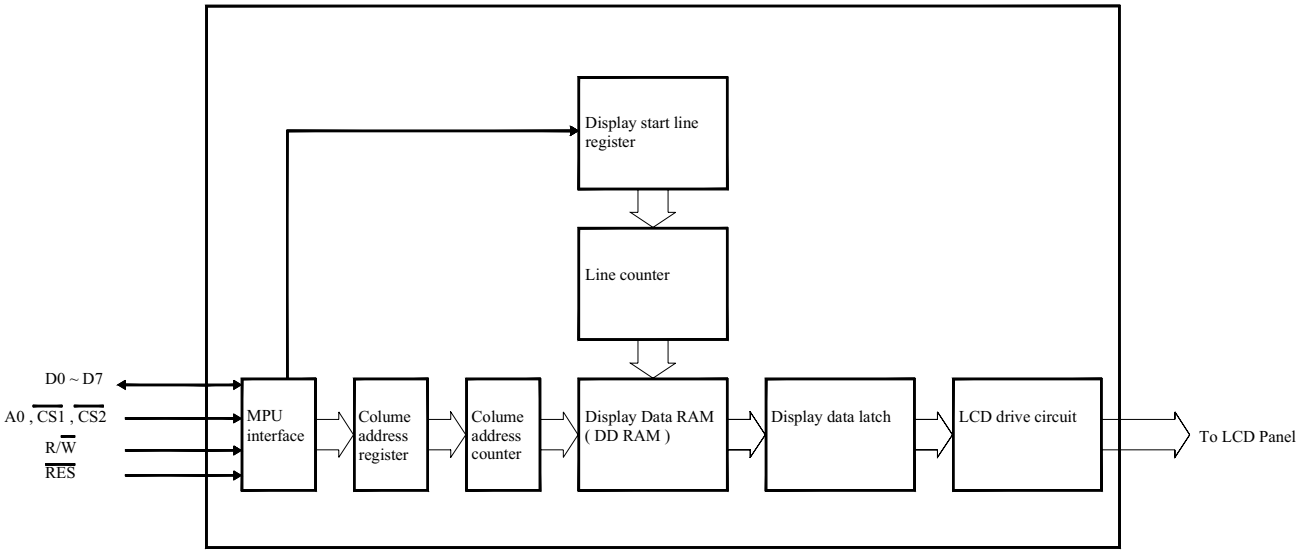
(10) Protect the module against static electricity and observe appropriate anti-static precautions.

12. Appendix (SED 1520 LSI controller)

12.1. Function Description

◆Block Diagram

This 122×32 dots LCD Module built in two SED 1520 LSI controller.



◆MPU interface

The SED 1520 controller transfers data via 8-bit bidirecional data buses (Do to D7), it can fit any MPU if it corresponds to SED 1520 Read and Write Timing Characteristics.

◆Data transfer

The SED1520 driver uses the A0, E and R/W signals to transfer data between the system MPU and internal registers, The combinations used are given in the table below.

A0	R/W	Function
1	1	Read display data
1	0	Write display data
0	1	Read status
0	0	Write to internal register (command)

◆Busy flag

When the Busy flag is logical 1, the SED1520 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (t_{CYC}) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

◆Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command.

◆Column Address Counter

The column address counter is a 7-bit presettable counter that supplies the column address for MPU access to the display data RAM. See Figure 1. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

◆Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 1.

◆Page Register

The page register is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 1. The contents of the page register are set by the Set Page Register

12.2 Commands Descriptions

Summary

Command	Code											Function
	A0	RD	WR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1:ON, 0:OFF
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	1	0	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address register.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1:Busy 0:Ready ADC 1:CW output 0:CCW output ON/OFF 1:Display off 0: Display on RESET 1:Being reset 0:Normal
Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
Read display data	1	0	1	Read data								Reads data from display RAM into data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0:CW output, 1:CCW output
Statis drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1:Static drive, 0:Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selets LCD duty cycle 1:1/32, 0:1/16
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Table 1

Table 1 is the command table. The SED 1520 series identifies a data bus using a combination of A0 and R/W (RD or WR) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

Display ON/OFF

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	1	0	1	1	1	D

AEH, AFH

This command turns the display on and off.

- D=1: Display ON
- D=0: Display OFF

Display Start Line

This command specifies the line address shown in Figure 1 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	0	A_4	A_3	A_2	A_1	A_0

C0H to DFH

This command loads display start line register.

A_4	A_3	A_2	A_1	A_0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 1.

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	1	1	1	0	A_1	A_0

B8H to BBH

This command loads the page address register.

A_1	A_0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 1.

Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0

00H to 4FH

This command loads the column address register.

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	0	0	1	1	1	1	79

Read Status

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n→segment driver n.
  ADC=0: Inverted. Column address 79-u→segment driver u.
- The ON/OFF bit indicates the current status of the display.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF
  ON/OFF=0: Display ON
- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

Write Display Data

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

Read Display Data

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	Read data							

Read 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.

After loading a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	1	0	0	0	0	D

AOH A1H

This command selects the relationship between display data RAM column addresses and segment drivers.

D=1: SEG0←column address 4FH,…….(inverted)

D=0: SEGO←column address 00H,…….(normal)

This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 1 for a table of segments and column addresses for the two values of D.

Static Drive ON/OFF

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	1	0	0	1	0	D

A4H A5H

Forces display on and all common outputs to be selected.

D=1: Static drive on

D=0: Static drive off

Select Duty

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	1	0	1	0	0	D

A8H A9H

This command sets the duty cycle of the LCD drive, Please set D=1, LCD duty cycle is 1/32 duty.

Read-Modify-Write

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	1	0	0	0	0	0

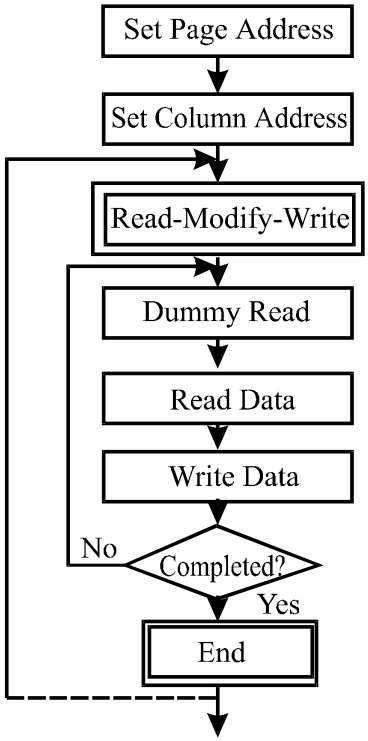
E0H

This command defeats column address register auto-increment after data reads. The current contents of the column address register are saved. This mode remains active until an End command is received.

• Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



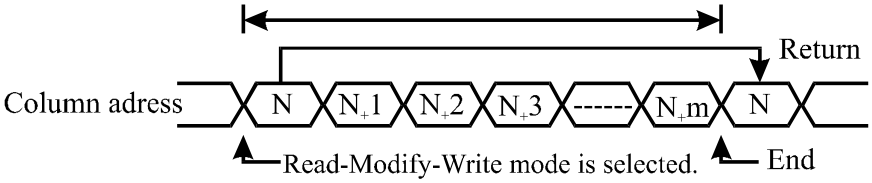
End

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

EEH

0	0	1	1	1	0	1	1	1	0

This command cancels read-modify-write mode and restores the contents of the column address regisster to their value prior to the receipt of the Read-Modify-Write command.



Reset

A_0	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	1	0	0	0	1	0

E2H

This command clears

- the display start line register.
- And set page address register to 3 page.

It does not affect the contents of the display data RAM.

When the power supply is turned on, a Reset signal is entered in the RES pin. The Reset command cannot be used instead of this Reset signal.

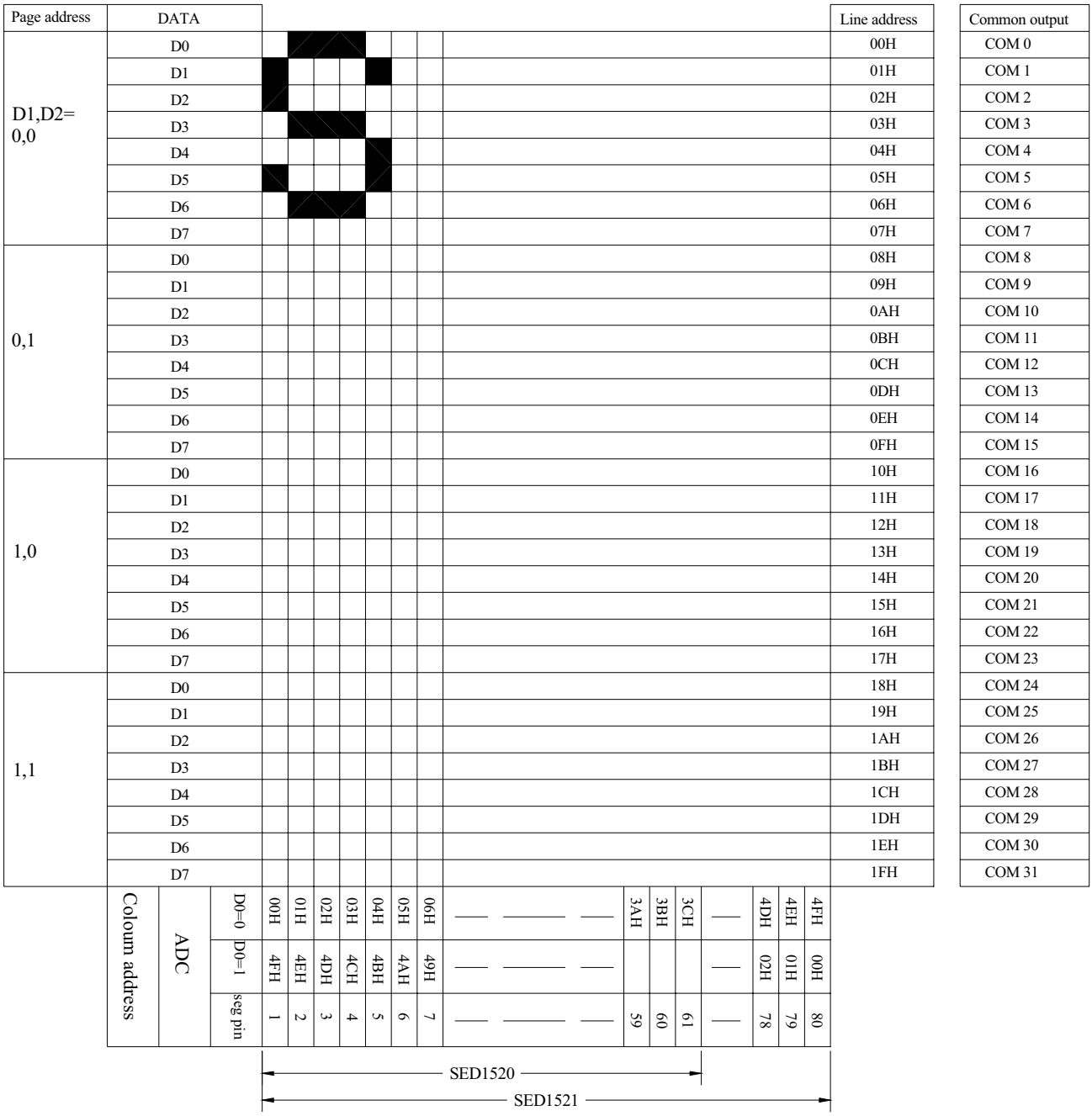


Figure 1. Display Data RAM Address

* The 122*32 dots display area is consist of two 61*32, The interface control pin CS1 enable the left 61*32,CS2 enable the right 61*32.

Front transmissive view