

CUSTOMER :  
MODEL : MOG-98GB64F-S series  
DESCRIPTION : LCD MODULE

◆ CUSTOMER APPROVAL

	CHECKED	CHECKED	APPROVAL
APPROVAL			
REMARK			

◆ SUPPLIER APPROVAL

PREPARED	CHECKED	APPROVAL

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## 1. General Specification

### (1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	98 × 64	dots
Module Size (W x H x T)	35.5*28.0*2.3max-EL B/L 34.0 x 28.0 x 1.6max-No B/L	mm
View area	31.0(W) × 22.5(H)	mm
Dot size	0.268(W) × 0.318(H)	mm
Dot pitch	0.28(W) × 0.33(H)	mm

### (2) Controller IC: PCF8548 Controller

### (3) Temperature Range

	Normal	Wide
Operating	0 ~ +50°C	-20 ~ +70°C
Storage	-10 ~ +60°C	-40 ~ +85°C

## 2. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage For Logic	VDD-VSS	-0.5	—	6.5	V
Supply Voltage For LCD	VLCD	0	—	16.0	V
Input Voltage	VI	-0.3	—	VDD+0.3	V
Operating Temperature	TOP	-20	—	+70	°C
Storage Temperature	TSTG	-30	—	+85	°C

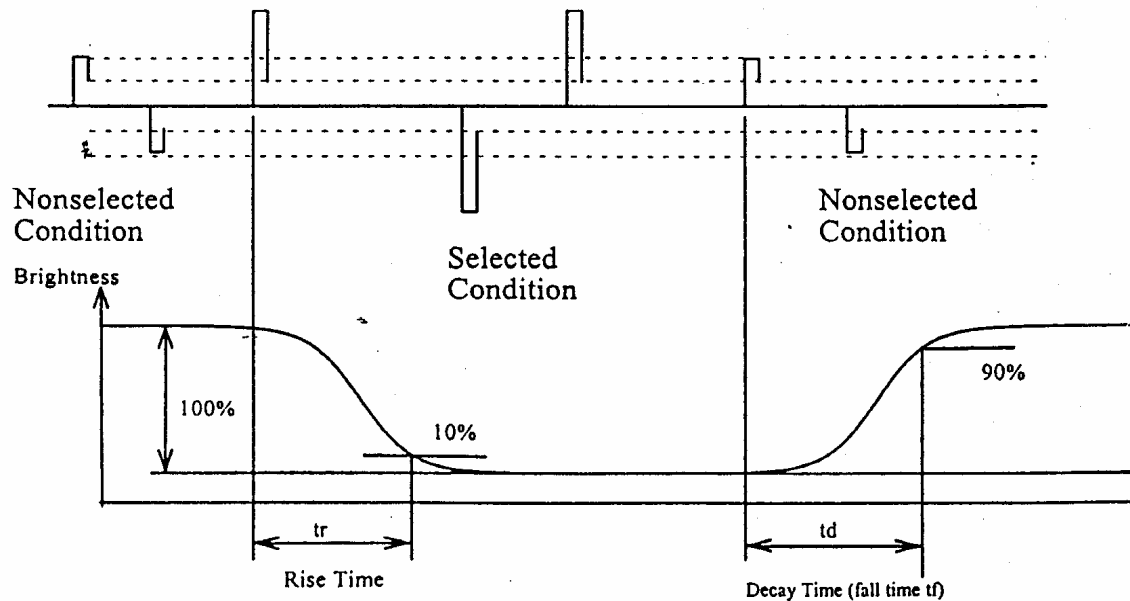
### 3. Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
<b>----- Electronic Characteristics -----</b>							
Logic Circuit Supply Voltage	VDD-VSS	--	2.7	3.0	5.5	V	
LCD Driving Voltage	VLCD	-20 °C	--	9.2	--	V	* It should be defined by real design.
		25 °C	--	<b>8.2</b>	--		
		+70 °C	--	7.2	--		
Input Voltage	VIH	--	0.7 VDD	--	VDD	V	
	VIL	--	0	--	0.3 VDD	V	
Logic Supply Current	IDD	VDD = 5V	--	0.3	--	mA	
<b>----- Optical Characteristics -----</b>							
Contrast	CR	-20 °C	--	1.7*	--		Note 1 * It should be defined by real design.
		25 °C	--	8*	--		
		70 °C	--	4.6*	--		
Rise Time	tr	-20 °C	--	2100*	--	ms	Note 2 * It should be defined by real design.
		25 °C	--	150*	--		
		70 °C	--	50*	--		
Fall Time	tf	-20 °C	--	5500*	--	ms	
		25 °C	--	250*	--		
		70 °C	--	65*	--		
Viewing Angle Range	$\theta f$	25°C & CR≥2	--	40	--	Deg.	Note 3
	$\theta b$		--	30	--		
	$\theta l$		--	35	--		
	$\theta r$		--	35	--		
Frame Frequency	fF	25°C	--	64	--	Hz	

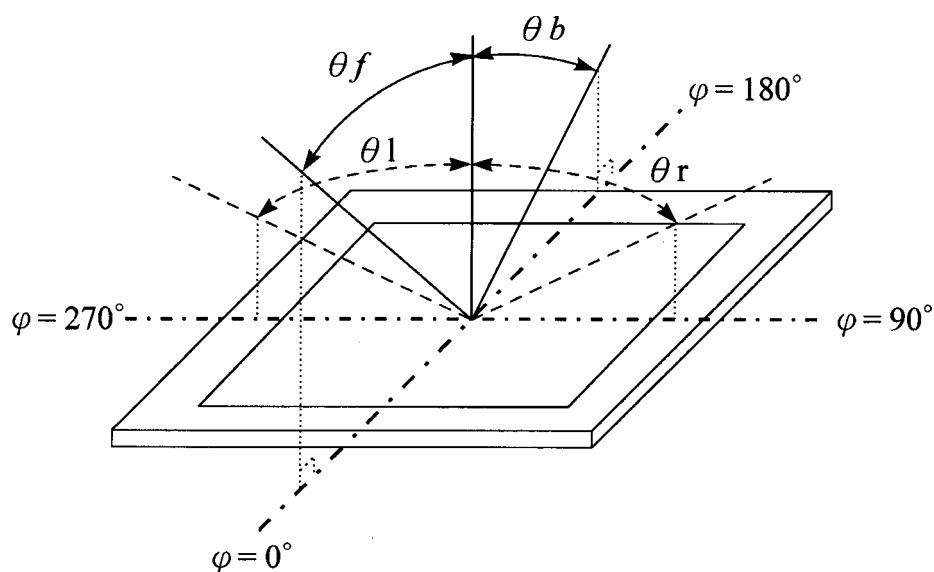
(NOTE 1) Contrast ratio :

$$CR = (\text{Brightness in OFF state}) / (\text{Brightness in ON state})$$

(NOTE 2) Response time :



(NOTE 3) Viewing angle



## 4. Interface Pin Function

No.	Symbol	Function
1	VLCD	LCD power supply
2	VSS1,VSS2	Logic ground 0V
3	VSS1,VSS2	Logic ground 0V
4	SCL	I <sup>2</sup> C-bus Serial clock signal input
5	SD	I <sup>2</sup> C-bus data lines
6	RES	This signal is used to rest the device. This signal is active Low.
7	VDD	Positive power supply
8	VDD	Positive power supply

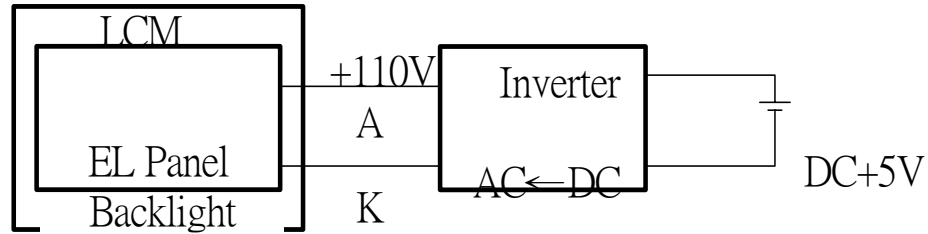
## 5. Backlight Information

EL /White( blue)

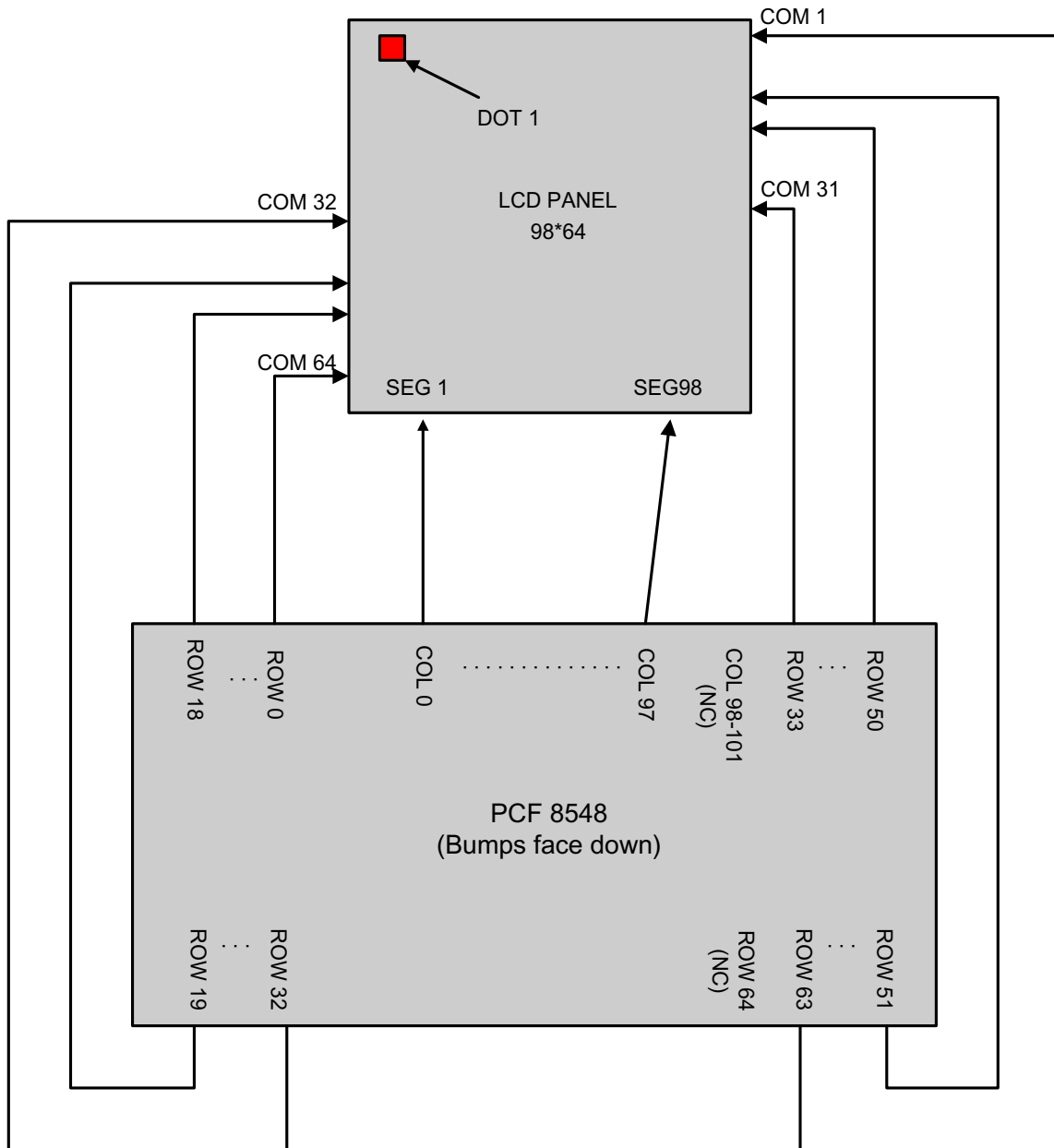
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Voltage	Vrms	--	110 (AC)		V	
Frequency	HZ	--	400		Hz	
Brightness*(Measure on LCD)	cd/m <sup>2</sup>	5	10		cd/m <sup>2</sup>	110Vrms 400Hz
CIE Chromaticity Diagram	X	--	0.2901 white 0.182 blue		--	
	Y	--	0.3608 white 0.46 blue		--	
Current Dissipation	mA/cm <sup>2</sup>	--	1.33		mA	
Power Dissipation	mW/cm <sup>2</sup>	--	26.29		mW	
Color	White(Blue)					

## 5.2 Backlight driving methods

E/L B/L driven from PINS of EL backlight directly



## 6. Block Diagram



### Display Configuration Setting :

**MX=0    MY=1**

**BRS=1    TRS=0**

## 7. Timing Characteristics

$V_{DD1} = 1.9$  to  $5.5$  V;  $V_{DD2}$  and  $V_{DD3} = 2.4$  to  $4.5$  V;  $V_{SS1}$  and  $V_{SS2} = 0$  V;  $V_{LCD} = 4.5$  to  $9$  V;  $T_{amb} = -40$  to  $+85$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{OSC}$	oscillator frequency	$V_{DD1} = 2.8$ V; $T_{amb} = -20$ to $+70$ °C	20	38	70	kHz
$f_{clk(ext)}$	external clock frequency		20	38	100	kHz
$f_{frame}$	frame frequency	$f_{OSC}$ or $f_{clk(ext)} = 38$ kHz; note 1	–	73	–	Hz
$t_{VHRL}$	$V_{DD1}$ to $\overline{RES}$ LOW	see Fig.17 and note 2	0	–	1	$\mu$ s
$t_{W(RES)}$	$\overline{RES}$ LOW pulse width	see Fig.17 and note 3	100	–	–	ns
<b>I<sup>2</sup>C-bus timing characteristics; see note 4</b>						
$f_{SCLK}$	SCL clock frequency		0	–	400	kHz
$t_{SCLL}$	SCL clock LOW period		1.3	–	–	$\mu$ s
$t_{SCLH}$	SCL clock HIGH period		0.6	–	–	$\mu$ s
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	0.9	$\mu$ s
$t_r$	SCL and SDA rise time	note 5	$20 + 0.1C_b$	–	300	ns
$t_f$	SCL and SDA fall time	note 5	$20 + 0.1C_b$	–	300	ns
$t_f(SDA)(ro)$	SDA fall time for read out	$V_{DD1} = <3.6$ V	$20 + 0.1C_b$	–	1000	ns
$C_b$	capacitive load represented by each bus line		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	$\mu$ s
$t_{HD;STA}$	START condition hold time		0.6	–	–	$\mu$ s
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	$\mu$ s
$t_{SW}$	tolerable spike width on bus	note 6	–	–	50	ns
$t_{BUF}$	bus free time between a STOP and START condition		1.3	–	–	$\mu$ s

### Notes

- $f_{frame} = \frac{f_{clk(ext)}}{520}$
- $\overline{RES}$  may be LOW before  $V_{DD1}$  goes HIGH.
- If  $t_{W(RES)}$  is longer than 3 ns (typical) a reset may be generated.
- All timing values are valid within the operating supply voltage and ambient temperature ranges and are referenced to  $V_{IL}$  and  $V_{IH}$  with an input voltage swing of  $V_{SS}$  to  $V_{DD}$ .
- The rise and fall times specified here refer to the driver device (i.e. not PCF8548) and are part of the general fast I<sup>2</sup>C-bus specification. When PCF8548 asserts an acknowledge on SDA, the minimum fall time is 10 ns.  
 $C_b$  = capacitive load per bus line.
- The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width  $t_{SW(max)}$ .

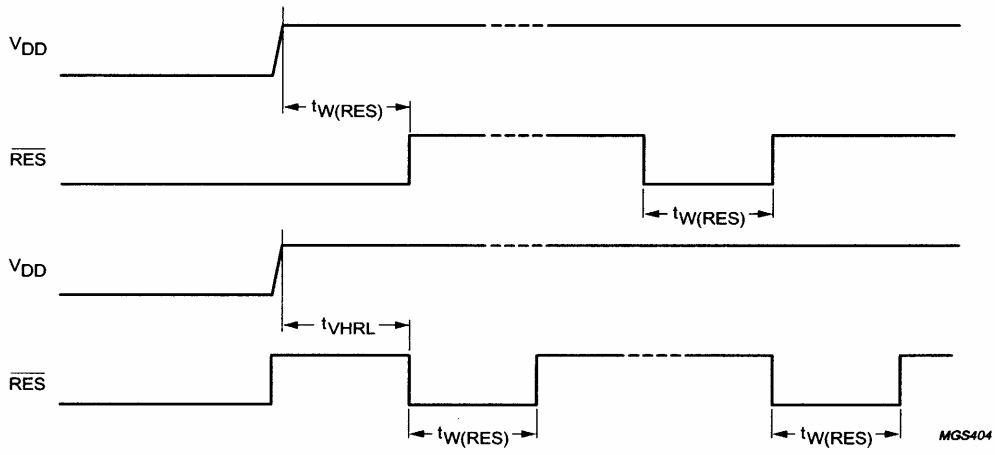


Fig.17 Reset timing.

## 8. Quality

### 8-1 Test Conditions

Tests should be conducted under the following conditions :

Ambient temperature :  $25 \pm 5^{\circ}\text{C}$

Humidity :  $60 \pm 25\% \text{ RH}$ .

### 8-2 Sampling Plan

Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

### 8-3 Acceptable Quality Level

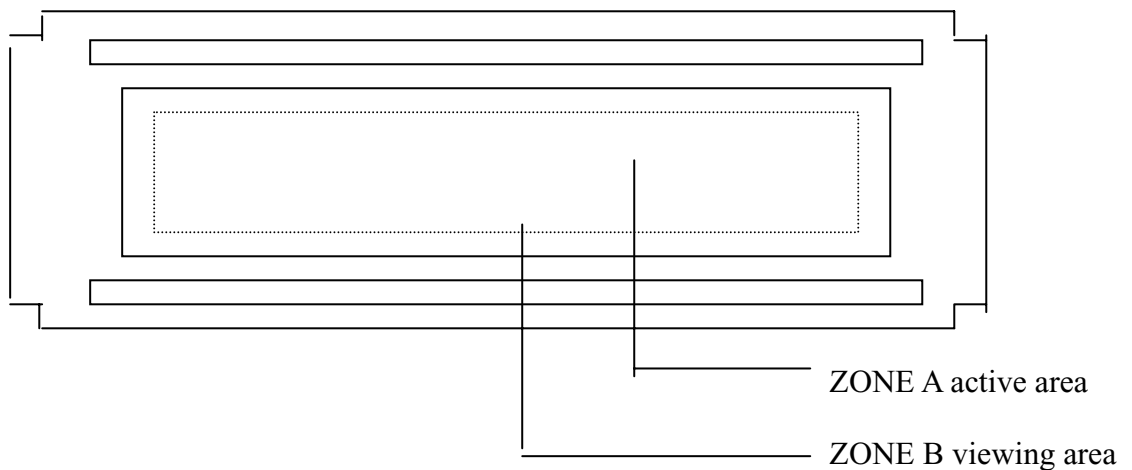
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

### 8-4 Appearance

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under fluorescent light. The inspection area of LCD panel shall be within the range of following limits.

## 8-5 Inspection Quality Criteria

Item	Description of defects			Class of Defects	Acceptable level (%)
Function	Short circuit or Pattern cut			Major	0.65
Dimension	Deviation from drawings			Major	1.5
Black spots	Ave . dia . D	area A	area B	Minor	2.5
	$D \leq 0.2$	Disregard			
	$0.2 < D \leq 0.3$	3	4		
	$0.3 < D \leq 0.4$	2	3		
	$0.4 < D$	0	1		
Black lines	Width W, Length L	A	B	Minor	2.5
	$W \leq 0.03$	disregard			
	$0.03 < W \leq 0.05$	3	4		
	$0.05 < W \leq 0.07, L \leq 3.0$	1	1		
	See line criteria				
Bubbles in polarizer	Average diameter D $0.2 < D < 0.5$ mm for N = 4 , D > 0.5 for N = 1			Minor	2.5
Color uniformity	Rainbow color or newton ring.			Minor	2.5
Glass Scratches	Obvious visible damage.			Minor	2.5
Contrast ratio	See note 1			Minor	2.5
Response time	See note 2			Minor	2.5
Viewing angle	See note 3			Minor	2.5



## 9. Reliability

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 min. 5 min. 30 min. ( 1 cycle ) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency : 10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

## 10. Handling Precautions

- (1) An LCD module is a fragile item and should not be subjected to strong mechanical shocks.
- (2) Avoid applying pressure to the module surface. This will distort the glass and cause a change in colour.
- (3) Under no circumstances should the position of the bezel tabs or their shape be modified.
- (4) Do not modify the display PCB in either shape or positioning of components.
- (5) Do not modify or move location of the zebra or heat seal connectors.
- (6) The device should only be soldered to during interfacing. Modification to other areas of the board should not be carried out.
- (7) In the event of LCD breakage and resultant leakage of fluid do not inhale, ingest or make contact with the skin. If contact is made rinse immediately.
- (8) When cleaning the module use a soft damp cloth with a mild solvent, such as Isopropyl or Ethyl alcohol. The use of water, ketone or aromatic is not permitted.
- (9) Prior to initial power up input signals should not be applied.
- (10) Protect the module against static electricity and observe appropriate anti-static precautions.

